

**Abstract 9 – Paper ID: 124****A Progressive Shortest-Path Routing Approach for 3D Mesh-Based Topologies with Supplementary 2D Links**Abhijit Biswas<sup>1</sup>, Sourish Dhar<sup>1</sup><sup>1</sup>Computer Science and Engineering, Assam University, Silchar, Assam, India*Email: abhi.021983@gmail.com***Abstract**

The development of 3D Network-on-Chip (NoC) architectures marks a major advancement in integrated circuit design, addressing the scaling limitations faced by traditional 2D NoCs. The pioneering academic work on 3D NoC surfaced around 2006, blending 3D integration—stacking multiple active silicon layers—with network-on-chip communication fabrics to boost system performance, bandwidth, and scalability.

Attempts to reduce 2D network diameter always invariably introduces supplementary links between corner nodes or to nodes in the middle. As is seen in the case of 2D mesh. Many variants such as 2D torus, diagonally connected mesh, C2 mesh, C mesh, diametrical mesh, XD mesh and torus heavily rely on adding supplementary links. These links do somewhat solve the issue at the cost of scalability in the 2D plane.

We evaluate a mesh-based 3D topology augmented with supplementary 2D links formed by vertically stacking and scaling the network along the Z-axis. Four supplementary links connect the four corner nodes to four central (middle-region) nodes in each 2D mesh plane. These links are invoked when the 2D routing distance exceeds  $N$  in an  $N \times N \times NN$  3D mesh ( $N \geq 4$ ), as they always provide a shortest path of less than  $NNN$  hops in the 2D plane.

The proposed progressive shortest-path routing algorithm computes the shortest distance from the source to a node with a supplementary link and from the destination to the corresponding node. Once the minimum 2D distance is achieved, the packet is routed through that node. If the source and destination lie in the same plane, delivery is completed within the plane; otherwise, the packet is forwarded along the Z-axis—either upward or downward—to reach the destination plane and final node.

The 3D network has been simulated and found to be generating only the shortest path and have incurred an average latency of  $20 \times 10^{-6}$  Seconds for  $5 \times 5 \times 5$  network size and an average latency of  $12.587 \times 10^{-6}$  Seconds for  $4 \times 4 \times 4$  network size.

**Keywords:** 3D Network-on-Chip, System-on-Chip, Latency, Hop count, Mesh topology